ABSTRACT

[0064] An imager with a multiplexer located at the pixel output line connected to associated column sample and hold circuitry. The multiplexer ensures that signals from pixels within a column are output to the correct output channels in the readout path. By having the multiplexer at the pixel output line, before any sample and hold circuitry, the imager can use simplified column select circuitry when signals are being read out to the output channels. As such, parasitic capacitance at the readout path is reduced, which produces faster readout speeds than typical imagers. In addition, the imager achieves lower readout noise and less power consumption than typical imagers.